NOTICE OF REV	Form Approved OMB No. 0704-0188				
Public reporting burden for this collection is estimated to searching existing data sources, gathering and maintaini information. Send comments regarding this burden estir suggestions for reducing this burden, to Department of Department of Education and Reports, 1215 Jefferson Davis Highway, and Budget, Paperwork Reduction Project (0704-0188), COMPLETED FORM TO EITHER OF THESE ADDRE ISSUING CONTRACTING OFFICER FOR THE CONT	2. PROCURING ACTIVITY NO.				
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	Defense Electronics Suppl	y Center	67268	5962-R024-94	
a. TYPED NAME (First, Middle Initial, Last)	1507 Wilmington Pike Dayton, OH 45444-5270		7. CAGE CODE 67268	8. DOCUMENT NO. <b>5962-88627</b>	
9. TITLE OF DOCUMENT		10. REVISION	LETTER	11. ECP NO.	
MICROCIRCUIT, DIGITAL, BIPOLAR, ADVANC	•	a. CURRENT	b. NEW	_	
8-BIT BINARY COUNTER, MONOLITHIC SILIC	JN.	Α	В		
12. CONFIGURATION ITEM (OR SYSTEM) TO WHIC	H ECP APPLIES				
13. DESCRIPTION OF REVISION					
Sheet 1: Revisions Itr column; add "B". Revisions description column; add "Chan, Revisions date column; add "93-11-19". Revision level block; change from "A" to "Rev status of sheets; for sheets 1, 2, and Sheet 2: 1.4 Recommended operating condition and substitute "9.5 ns". 1.4 Recommended operating conditions, and substitute "12.5 ns". 1.4 Recommended operating conditions, and substitute "1.0 ns". 1.4 Recommended operating conditions, and substitute "1.0 ns". 1.5 Revision level block; change from "A" to "Change from "A"	B". 14 change from "A" to "B". Sh ns, setup time: PE to CP setup time: U/D to CP, hold time: Pn to CP, de hold time: CET, CEP to CP: - B". groups 10 and 11, minimum co but not tested".	eets 4 and 5 add -, delete "7.5 ns" delete "7.5 ns" elete "0 ns", delete "1.0 ns			
14. THIS SECTION FOR GOVERNMENT USE C					
a. (X one) X (1) Existing docum	ent supplemented by the NOF	R may be used in	manufacture.		
(2) Revised docum	nent must be received before r	nanufacturer may	incorporate this char	nge.	
(3) Custodian of m	aster document shall make ab	ove revision and	furnish revised docur	nent.	
b. ACTIVITY AUTHORIZED TO APPROVE CHANGE	FOR GOVERNMENT	c. TYPED NAME	(First, Middle Initial, Las	it)	
DESC-ECC			Monica L. Poel	king	
d. TITLE	e. SIGNATURE		f. DATE SIGNED (Y'	YMMDD)	
Chief, Custom Microelectronics	Monica L. Poelk	ing	g	93-11-19	
15a. ACTIVITY ACCOMPLISHING REVISION	b. REVISION COMPLETED (Si	gnature)	c. DATE SIGNED (YYMMDD)		
DESC-ECC	Larry T. Gauder		93-11-19		

# 13. DESCRIPTION OF REVISION - CONTINUED

Document No.: 5962-88627

Revision: B

NOR No.: 5962-R024-94

Sheet: 2 of 2

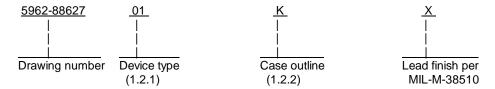
Sheet 14. add "2/" to 5962-8862701KX and 5962-88627013X. add "2/ Not available from an approved source". delete company name and address and substitute the following: "Phillips Semiconductor 811 E. Arques Avenue Sunnyvale, CA 94088-3409" Revision level block; change from "A" to "B".

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DESC FORM 193 SEP 87

#### 1. SCOPE

- 1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".
  - 1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 <u>Device type(s)</u>. The device type(s) shall identify the circuit function as follows:

Device type	<u>Generic number</u>	Circuit function
01	54F269	8-bit bidirectional binary counter

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
----------------	--------------

- Κ F-6 (24-lead, .640" x .420" x .090"), flat package
- D-9 (24-lead, 1.280" x 0.310" x 0.200"), dual-in-line package L
- C-4 (28-terminal, .460" x .460" x .100"), square chip carrier package
- 1.3 Absolute maximum ratings.

```
Storage temperature range ----- -65° C to +150° C
Maximum power dissipation (P<sub>D</sub>) 1/ ----- 69 mW
Lead temperature (soldering, 10 seconds) --- +300°C
Thermal resistance, junction-to-case (\Theta_{JC}) -- See MIL-M-38510, appendix C Junction temperature (T_J) ------+175 ^{\circ} C
```

1.4 Recommended operating conditions.

Supply voltage range ( $V_{CC}$ ) Case operating temperature range ( $T_C$ ) Minimum high level input voltage ( $V_{IH}$ ) Maximum low level input voltage ( $V_{IL}$ ) Minimum high or low setup time ( $t_s$ ):	2.0 V dc
Pn to CP	
CET, CEP to CP	10.5 ns
Minimum high or low hold time (t <sub>h</sub> ):  Pn to CP	
<u>Pn</u> to CP <u>PE</u> to <u>CP</u>	
CET, CEP to CP	
Minimum high or low clock pulse width $(t_w)$	

 $\underline{1}$ / Must withstand the added P<sub>D</sub> due to the short circuit test; e.g.,  $I_{OS}$ .

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#### 2. APPLICABLE DOCUMENTS

2.1 <u>Government specification, standard, and bulletin</u>. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

**SPECIFICATION** 

**MILITARY** 

MIL-M-38510 - Microcircuits, General Specification for.

**STANDARD** 

**MILITARY** 

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

**MILITARY** 

MIL-BUL-103 - List of Standardized Military Drawing (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

## 3. REQUIREMENTS

- 3.1 <u>Item requirements</u>. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.
- 3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.
  - 3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.
  - 3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.
  - 3.2.3 Truth table. The truth table shall be as specified on figure 2.
  - 3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.
  - 3.2.5 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 4.
- 3.3 <u>Electrical performance characteristics</u>. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.
- 3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

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		TABLE I. Electrical performance charac	teristics.			
Test	  Symbol 	   Conditions   -55° C ≤ T <sub>C</sub> ≤ +125° C   unless otherwise specified	   Group A  subgroups	   <u>Limits</u>       Min   Max		   Unit 
High level output	    V <sub>ОН</sub>	   V <sub>CC</sub> = 4.5 V, V <sub>II</sub> = 0.8 V	1, 2, 3	2.5		   V
voltage		V <sub>IH</sub> = 2.0 V, I <sub>OH</sub> = -1.0 mA		 		
Low level output voltage	IV <sub>OL</sub>	$ V_{CC}  = 4.5 \text{ V}, V_{IL} = 0.8 \text{ V}$ $ V_{IH}  = 2.0 \text{ V}, V_{OL}  = 20 \text{ mA}$	1, 2, 3	   	0.5	V   
Input clamp voltage	V <sub>IC</sub>	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA	1, 2, 3	 	-1.2	V 
High level input current	I <sub>IH1</sub>	$V_{CC} = 5.5 \text{ V}, V_{IN} = 7.0 \text{ V}$	1, 2, 3	 	100	μA 
	I <sub>IH2</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V	1, 2, 3	 	20	μΑ 
Low level input current	<sub>  </sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V	1, 2, 3	i 	-0.6	mA 
Short circuit output _current	los	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 0.0 V <u>1</u> /	1, 2, 3	-60   	-150 	mA 
Supply current	IICCH         	V <sub>CC</sub> = 5.5 V   PE = CET = CEP = <u>U</u> /D = GND   Pn = 4.5 V, CP = _/   outputs open	1, 2, 3       		120       	mA       
	  I <sub>CCL</sub>   	V <sub>CC</sub> = <u>5.5</u> V   PE = C <u>ET</u> = CEP = U/D = GND   CP = _/ outputs open	1, 2, 3	     	  125   	mA     
Maximum clock frequency	  f <sub>MAX</sub> 	$ V_{CC}  = 5.0 \text{ V}$ $ C_{L}  = 50 \text{ pF}$ $ R_{L}  = 500\Omega$	   <u>9</u>    10,11	  100     85		   MHz 
Propagation delay time, CP to Qn (load)	  t <sub>PLH1</sub>	See figures 3 and 4	   <u>9</u> 	3.5	9	   ns
, ,	<u> </u> 	_	10, 11 	3.5	10 	<del> </del>
	İt <sub>PHL1</sub>		<u>  9</u> 	4	8.5	ns
		<u> </u>	10, 11	4	9	

See footnote at end of table.

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	TABL	E I. Electrical performance	characteristics	<u>s</u> - Continued	l.		
Test	  Symbol	Conditions	   Group A	Limits		   Unit	
		$-55^{\circ}$ C $\leq$ T <sub>C</sub> $\leq$ +125 $^{\circ}$ C unless otherwise specif	subgroups ied	   	   Min 	   Max 	
Propagation delay time,	  t <sub>PLH2</sub>	V <sub>CC</sub> = 5.0 V		9	3.5	8.0	ns
CP to Qn (count)	<u> </u>	$ C_L  = 50 \text{ pF}$ $ R_L  = 500\Omega$	PE = 2.0 V	   10, 11	3.5	9.0	<u> </u>
	  t <sub>PHL2</sub>	See figures 3 and 4 		   <u>9</u>	   4.5	  10.5	   ns
		<u> </u>	 	  10, 11	   4.5	  11.0	 
Propag <u>atio</u> n delay time, CP to TC	  t <sub>PLH3</sub>			j   9	4.5	9.5	   ns
CP to TC		 <u> </u>		l <u>  10, 11</u>	4.5	1 10.5	
	  t <sub>PHL3</sub>	<u> </u>		   <u>9</u>	   6.0	10.0	   ns
	 	 <u> </u>		 <u>  10, 11</u>	   5.5	  10.5	<u> </u>
Pr <u>opa</u> ga <u>tion</u> delay time, CET to TC	  t <sub>PLH4</sub>			   <u>9</u>	3.5	9.0	   ns
CETIOTC	<u></u>	 		10, 11	3.5	10.5	<u> </u>
	l <sup>[t</sup> PHL4	<u> </u>		   <u>9</u>	3.0	10.5	   ns
		<u> </u> _		   <u>10, 11</u>	3.0	   11.5	
Prop <u>ag</u> ati <u>on</u> delay time,	  t <sub>PLH5</sub>			   <u>9</u>	3.5	9.5	   ns
U/D to TC	<u> </u>	 _		   <u>10, 11</u>	   3.5	  10.0	<u> </u>
	  t <sub>PHL5</sub>			   <u>9</u>	   4.5	   9.5	   ns
		] 		  10, 11	   4.5	  11.0	

 $<sup>\</sup>underline{1}/$  Not more than one output should be shorted at a time, and the duration of the short circuit condition should not exceed 1 second.

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  Case  outlines 	     K and L 	3
  Terminal   <u>number</u>	   Terminal   symbol	
		NC   V/D   Q <sub>0</sub>   Q <sub>1</sub>   Q <sub>2</sub>   Q <sub>3</sub>   QC   NC   NC   CEP   CEC   CC   P <sub>7</sub>   P <sub>6</sub>   CC   P <sub>7</sub>   P <sub>8</sub>   CC   P <sub>8</sub>   P <sub></sub>
24   25   26   27	PE     	P <sub>3</sub>   P <sub>2</sub>   P <sub>1</sub>   P <sub>0</sub>
28		PE

NC = No connection

FIGURE 1. Terminal connections.

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   Pin 	   Pin description   
<u> </u>	Parallel data inputs
į <u> </u>	Parallel enable input (active LOW)
CEP	Count enable parallel input (active LOW)
CET	Count enable trickle input (active LOW)
CP	Clock input
TC	
Q <sub>0</sub> - Q <sub>7</sub>	   Flip-flop outputs 

FIGURE 1. <u>Terminal connections</u> - Continued.

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     Operating	   	   Inputs					   Outputs   	
mode   	  CP 	  U/D 	  CEP 	  CET 	  PE 	<u> </u>	   Q <sub>n</sub> 	  TC   
   Parallel   load 	  ↑  ↑	   X   X	   X   X 	  X  X 	       	  I  h 	   L   H 	  (a)    (a)
   Count   up	  ↑  ↑ 	   h 	       	        	  h   	:	  Count  up 	  (a)   
   Count   down	  ↑  ↑ 	 	 	        	  h   	  X   	  Count  down 	  (a)
   Hold   do nothing 	  1  1	   X   X 	  h  X 	   X   h 	  h  h 	  X  X 	   qn   qn 	  (a)     H

H = High voltage level steady state.

h = High voltage level one setup time prior to the low-to-high clock transition.

L = Low voltage level steady state.

I = Low voltage level one setup time prior to the low-to-high clock transition.

X = Irrelevant

q = Lower case letters indicate the state of the referenced output prior to the low-to-high clock transition.

 $\uparrow$  = Low-to-high clock t<u>ran</u>sition.

(a) = The TC is low when CET is low and the counter is at terminal count. Terminal count up is with all  $\mathbf{Q}_{\mathbf{n}}$  outputs high and terminal count down is with all  $\mathbf{Q}_{\mathbf{n}}$  outputs low.

FIGURE 2. Truth table.

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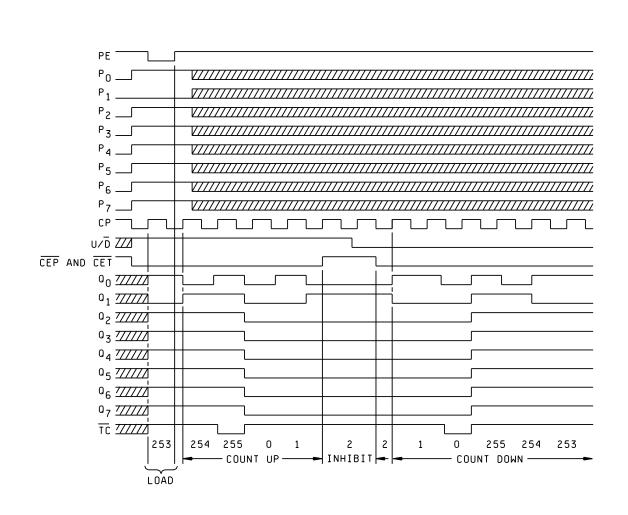


FIGURE 3. Timing diagram.

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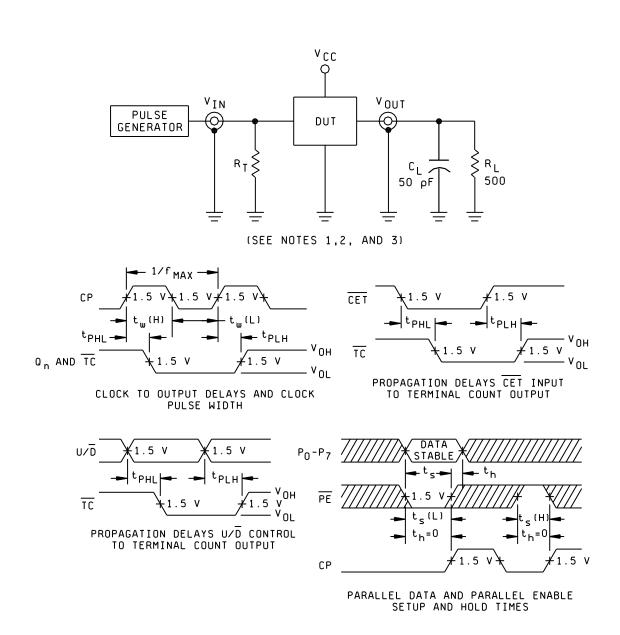
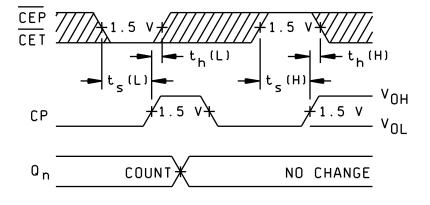
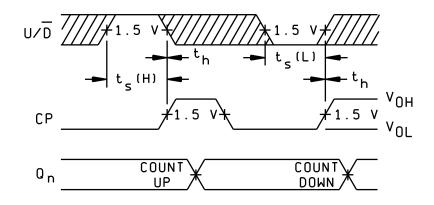


FIGURE 4. Test circuit and switching waveforms.

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COUNT ENABLE SETUP AND HOLD TIMES



UP/DOWN CONTROL SETUP AND HOLD TIMES

# NOTES:

- C<sub>L</sub> includes probe and jig capacitance.
   R<sub>T</sub> = Z<sub>OUT</sub> of pulse generators.
   Input pulse characteristics: PRR = 1 MHz, t<sub>TLH</sub> = t<sub>THL</sub> = 2.5 ns, duty cycle = 50%.
   The shaded areas indicate when the input is permitted to change for predictable output performance.

FIGURE 4. Test circuit and switching waveforms - Continued.

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- 3.5 <u>Marking</u>. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).
- 3.6 <u>Certificate of compliance</u>. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.
- 3.7 <u>Certificate of conformance</u>. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.
  - 3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).
- 3.9 <u>Verification and review</u>. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

### 4. QUALITY ASSURANCE PROVISIONS

- 4.1 <u>Sampling and inspection</u>. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).
- 4.2 <u>Screening</u>. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:
  - a. Burn-in test, method 1015 of MIL-STD-883.
    - (1) Test condition A, D, E, or F using the circuit submitted with the certificate of compliance (see 3.6 herein).
    - (2)  $T_A = +125^{\circ} C$ , minimum.
  - b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.
- 4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.
  - 4.3.1 Group A inspection.
    - a. Tests shall be as specified in table II herein.
    - b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
    - c. Subgroups 7 and 8 tests shall include verification of the truth table.

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### 4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
  - (1) Test condition A, D, E, or F using the circuit submitted with the certificate of compliance (see 3.6 herein).
  - (2)  $T_A = +125^{\circ}C$ , minimum.
  - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups   (per method   5005, table I)
Interim electrical parameters (method 5004)	
Final electrical test parameters (method 5004)	   1*, 2, 3, 7, 8   9, 10, 11
Group A test requirements (method 5005)	  1,2,3,7,8   9,10,11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

<sup>\*</sup> PDA applies to subgroup 1.

### 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

## 6. NOTES

- 6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.
- 6.2 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

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- 6.3 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).
- 6.4 <u>Record of users</u>. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-6022.
  - 6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8525.
- 6.6 <u>Approved source of supply</u>. An approved source of supply is listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendor listed in MIL-BUL-103 has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC. The approved source of supply listed below is for information purposes only and is current only to the date of the last action of this document.

   Military drawing   part number   	  Vendor  CAGE  number 	Vendor     similar part     number <u>1</u> /
5962-8862701KX	18324	54F269/BKA
5962-8862701LX	18324	54F269/BLA
   5962-88627013X	   18324 	   54F269/B3A 

1/ <u>Caution</u>. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

Vendor name and address

18324

Signetics Corporation 4130 South Market Court Sacramento, CA 95834

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MILITARY DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

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